CLAIMS

What is claimed is:

1. A method for fabricating a self-aligned gated field emission device, comprising:

providing a substrate having a surface and a predetermined thickness;

disposing a porous layer having a first surface and a first predetermined thickness on the surface of the substrate, wherein the porous layer defines a plurality of substantially cylindrical channels, the plurality of substantially cylindrical channels aligned substantially parallel to one another and substantially perpendicular to the surface of the substrate;

disposing a filler material within at least a portion of the substantially cylindrical channels defined by the porous layer to form a plurality of substantially rod-shaped structures;

selectively removing a portion of the porous layer to form a second surface and a second predetermined thickness of the porous layer;

disposing a gate dielectric layer having a surface and a predetermined thickness on the second surface of the porous layer and a portion of each of the plurality of substantially rod-shaped structures;

disposing a conductive layer having a predetermined thickness on the surface of the gate dielectric layer; and

selectively removing a portion of the conductive layer, the gate dielectric layer, and each of the plurality of substantially rod-shaped structures.

2. The method of claim 1, wherein the substrate comprises one of a semiconductor material and a metal.

3. The method of claim 2, wherein the semiconductor material comprises at least one of silicon, amorphous silicon, poly-silicon, silicon carbide and gallium nitride.

4. The method of claim 2, wherein the metal comprises at least one of Al, W and Nb.

5. The method of claim 1, wherein the thickness of the substrate is between about 1 micron and about 550 microns.

6. The method of claim 1, wherein the porous layer comprises an anodized metal oxide.

7. The method of claim 6, wherein the step of disposing the porous layer comprises:

providing a metal sheet;

mechanically deforming the metal sheet; and

anodizing the metal sheet to form the anodized metal oxide.

8. The method of claim 7, wherein the step of mechanically deforming the metal sheet comprises molding the metal sheet using a master stamp having a predetermined pattern.

9. The method of claim 6, wherein the step of disposing the porous layer comprises:

applying a thin layer of block copolymer to the surface of the substrate, wherein the block copolymer comprises a matrix phase and a cylinder phase;

aligning the cylinder phase perpendicular to the surface of the substrate;

curing the block copolymer;

removing the cylinder phase from the matrix phase to provide an ordered configuration that exposes selected areas of a metal on the surface of the substrate; and

anodizing the metal to form the anodized metal oxide.

10. The method of claim 6, wherein the step of disposing the porous layer comprises:

applying a radiation sensitive resist layer to the surface of the substrate;

degrading the radiation sensitive resist layer to form an ordered configuration of circular holes comprising degraded radiation sensitive resist in the radiation sensitive resist layer;

removing the degraded radiation sensitive resist to expose selected areas of a metal on the surface of the substrate; and

anodizing the metal to form the anodized metal oxide.

11. The method of claim 10, wherein the step of degrading the radiation sensitive resist layer comprises exposing the radiation sensitive resist layer to at least one of ultraviolet radiation, x-rays and an electron beam.

12. The method of claim 1, wherein the first thickness of the porous layer is between about 0.5 microns and about 5 microns.

13. The method of claim 6, wherein disposing the anodized metal oxide on the surface of the substrate comprises:

disposing a metal layer having a predetermined thickness on the surface of the substrate; and

reacting the metal layer to form the anodized metal oxide.

14. The method of claim 13, wherein the metal layer comprises at least one of Al and Ti.

15. The method of claim 6, wherein the step of disposing a metal layer having a predetermined thickness on the surface of the substrate comprises:

depositing a stress-relief layer on the surface of the substrate; and

disposing a metal layer having a predetermined thickness on the stress-relief layer.

16. The method of claim 15, wherein the stress-relief layer comprises Nb.

17. The method of claim 14, wherein the anodized metal oxide comprises at least one of anodized aluminum oxide and anodized titanium oxide.

18. The method of claim 13, wherein the thickness of the metal layer is between about 0.1 microns and about 50 microns.

19. The method of claim 1, wherein each of the plurality of substantially cylindrical channels has a diameter of between about 1 nm and about 1,000 nm.

20. The method of claim 19, wherein each of the plurality of substantially cylindrical channels has a diameter of between about 5 nm and about 50 nm.

21. The method of claim 1, wherein each of the plurality of substantially cylindrical channels has a length of between about 0.1 microns and about 5 microns.

22. The method of claim 1, wherein the filler material comprises at least one of a metal, a carbide and a combination thereof.

23. The method of claim 22, wherein the filler material comprises at least one of Pt, Mo, W, Ta, Ir, Mo_2C, HfC, ZrC, TaC, WC, SiC and NbC.

24. The method of claim 1, wherein the filler material comprises a dielectric material.

25. The method of claim 24, wherein the dielectric material comprises at least one metal oxide.

26. The method of claim 25, wherein the at least one metal oxide comprises at least one of TiO, TiO_2, ZnO, ZrO_2, Al_2O_3, Nb_2O_5, Cr_2O_3, $ZrTiO_4$, ZrO_2-Al_2O_3, Al_2O_3-Cr_2O_3, Al_2O_3-TiO_2, TiO_2-RuO_2 and a combination thereof.

27. The method of claim 24, further comprising reacting the dielectric material to form a plurality of substantially rod-shaped insulating non-metallic contact structures.

28. The method of claim 1, wherein each of the plurality of substantially rod-shaped structures has a diameter of between about 1 nm and about 60 nm.

29. The method of claim 1, wherein each of the plurality of substantially rod-shaped structures has a length of between about 0.1 microns and about 5 microns.

30. The method of claim 1, wherein selectively removing a portion of the porous layer comprises etching the porous layer.

31. The method of claim 1, wherein the second thickness of the porous layer is between about 0.5 microns and about 5 microns.

32. The method of claim 1, wherein the gate dielectric layer comprises a material selected from the group consisting of SiO_2, SiN_x, wherein $0.5 \leq x \leq 1.5$, and Al_2O_3.

33. The method of claim 1, wherein the thickness of the gate dielectric layer is between about 1 nm and about 25 nm.

34. The method of claim 1, wherein the conductive layer comprises a material selected from the group consisting of a metal and a semiconductor material.

35. The method of claim 34, wherein the metal comprises at least one of Nb, Pt, Al, W, Mo, Ti, Ni and Cr.

36. The method of claim 34, wherein the semiconductor material comprises at least one of Si, GaN, GaAs and SiC.

37. The method of claim 1, wherein the thickness of the conductive layer is between about 20 nm and about 100 nm.

38. The method of claim 1, wherein selectively removing a portion of the conductive layer, the gate dielectric layer, and each of the plurality of substantially

rod-shaped structures comprises ion milling a portion of the conductive layer, the gate dielectric layer, and each of the plurality of substantially rod-shaped structures.

39. The method of claim 1, wherein the steps of disposing the conductive layer on the surface of the gate dielectric layer and selectively removing a portion of the conductive layer are performed simultaneously.

40. A method for fabricating a self-aligned gated field emission device, comprising:

providing a semiconductor layer having a surface and a predetermined thickness;

disposing an anodized aluminum oxide layer having a first surface and a first predetermined thickness on the surface of the semiconductor layer, wherein the anodized aluminum oxide layer defines a plurality of substantially cylindrical channels, the plurality of substantially cylindrical channels aligned substantially parallel to one another and substantially perpendicular to the surface of the semiconductor layer;

disposing a filler material within at least a portion of the substantially cylindrical channels defined by the anodized aluminum oxide layer to form a plurality of substantially rod-shaped structures;

selectively removing a portion of the anodized aluminum oxide layer to form a second surface and a second predetermined thickness of the anodized aluminum oxide layer;

disposing a gate dielectric layer having a surface and a predetermined thickness on the second surface of the anodized aluminum oxide layer and a portion of each of the plurality of substantially rod-shaped structures;

disposing a conductive layer having a predetermined thickness on the surface of the gate dielectric layer; and

selectively removing a portion of the conductive layer, the gate dielectric layer, and each of the plurality of substantially rod-shaped structures.

41. The method of claim 40, wherein the semiconductor layer comprises at least one of silicon, amorphous silicon, poly-silicon, silicon carbide and gallium nitride.

42. The method of claim 40, wherein the thickness of the semiconductor layer is between about 1 micron and about 550 microns.

43. The method of claim 40, wherein the first thickness of the anodized aluminum oxide layer is between about 0.5 microns and about 5 microns.

44. The method of claim 40, wherein disposing the anodized aluminum oxide layer on the surface of the semiconductor layer comprises:

disposing an aluminum layer having a predetermined thickness on the surface of the semiconductor layer; and

reacting the aluminum layer to form the anodized aluminum oxide layer.

45. The method of claim 44, wherein the step of disposing an aluminum layer having a predetermined thickness on the surface of the substrate comprises:

depositing a stress-relief layer on the surface of the substrate; and

disposing an aluminum layer having a predetermined thickness on the stress-relief layer.

46. The method of claim 45, wherein the stress-relief layer comprises Nb.

47. The method of claim 44, wherein the thickness of the aluminum layer is between about 0.5 microns and about 50 microns.

48. The method of claim 40, wherein each of the plurality of substantially cylindrical channels has a diameter of between about 1 nm and about 60 nm.

49. The method of claim 40, wherein each of the plurality of substantially cylindrical channels has a length of between about 0.5 microns and about 5 microns.

50. The method of claim 40, wherein the filler material comprises at least one of a metal, a carbide and a combination thereof.

51. The method of claim 50, wherein the filler material comprises at least one of Pt, Mo, W, Ta, Ir, Mo_2C, HfC, ZrC and NbC.

52. The method of claim 40, wherein the filler material comprises a dielectric material.

53. The method of claim 52, wherein the dielectric material comprises at least one of TiO, TiO_2, ZnO, ZrO_2, Al_2O_3, Nb_2O_5, Cr_2O_3, $ZrTiO_4$, ZrO_2-Al_2O_3, Al_2O_3-Cr_2O_3, Al_2O_3-TiO_2, TiO_2-RuO_2 and a combination thereof.

54. The method of claim 52, further comprising reacting the dielectric material to form a plurality of substantially rod-shaped metallic contact structures.

55. The method of claim 40, wherein selectively removing a portion of the anodized aluminum oxide layer comprises etching the anodized aluminum oxide layer.

56. The method of claim 55, wherein the step of disposing the porous layer comprises:

providing a metal sheet;

mechanically deforming the metal sheet; and

anodizing the metal sheet to form the anodized metal oxide.

57. The method of claim 56, wherein the step of mechanically deforming the metal sheet comprises molding the metal sheet using a master stamp having a predetermined pattern.

58. The method of claim 55, wherein the step of disposing the porous layer comprises:

applying a thin layer of block copolymer to the surface of the substrate, wherein the block copolymer comprises a matrix phase and a cylinder phase;

aligning the cylinder phase perpendicular to the surface of the substrate;

curing the block copolymer;

removing the cylinder phase from the matrix phase to provide an ordered configuration that exposes selected areas of a metal on the surface of the substrate; and

anodizing the metal to form the anodized metal oxide.

59. The method of claim 55, wherein the step of disposing the porous layer comprises:

applying a radiation sensitive resist layer to the surface of the substrate;

degrading the radiation sensitive resist layer to form an ordered configuration of circular holes comprising degraded radiation sensitive resist in the radiation sensitive resist layer;

removing the degraded radiation sensitive resist to expose selected areas of a metal on the surface of the substrate; and

anodizing the metal to form the anodized metal oxide.

60. The method of claim 59, wherein the step of degrading the radiation sensitive resist layer comprises exposing the radiation sensitive resist layer to at least one of ultraviolet radiation, x-rays and an electron beam.

61. The method of claim 40, wherein the second thickness of the anodized aluminum oxide layer is between about 0.5 microns and about 5 microns.

62. The method of claim 40, wherein the dielectric layer comprises a material selected from the group consisting of SiO_2, SiN_x, wherein $0.5 \leq x \leq 1.5$, and Al_2O_3.

63. The method of claim 40, wherein the thickness of the gate dielectric layer is between about 1 nm and about 25nm.

64. The method of claim 40, wherein the conductive layer comprises a material selected from the group consisting of a metal and a semiconductor material.

65. The method of claim 64, wherein the metal comprises at least one of Nb, Pt, Al, W, Mo, Ti, Ni and Cr.

66. The method of claim 64, wherein the semiconductor material comprises at least one of Si, GaN, GaAs and SiC.

67. The method of claim 40, wherein the thickness of the conductive layer is between about 20 nm and about 100 nm.

68. The method of claim 40, wherein selectively removing a portion of the conductive layer, the gate dielectric layer, and each of the plurality of substantially rod-shaped structures comprises ion milling a portion of the conductive layer, the gate dielectric layer, and each of the plurality of substantially rod-shaped structures.

69. A self-aligned gated field emission device, comprising:

a substrate having a surface and a predetermined thickness;

a porous layer having a surface and a predetermined thickness disposed adjacent to the surface of the substrate, wherein the porous layer defines a plurality of substantially cylindrical channels, each of the plurality of substantially cylindrical channels aligned substantially parallel to one another and substantially perpendicular to the surface of the substrate;

a plurality of substantially rod-shaped structures disposed within at least a portion of the plurality of substantially cylindrical channels defined by the porous layer and adjacent to the surface of the substrate, wherein a portion of each of the plurality of substantially rod-shaped structures protrudes above the surface of the porous layer;

a gate dielectric layer having a surface and a predetermined thickness disposed on the surface of the porous layer, wherein the gate dielectric layer is disposed between the plurality of substantially rod-shaped structures; and

a conductive layer having a predetermined thickness selectively disposed on the surface of the gate dielectric layer, wherein the conductive layer is selectively disposed between the plurality of substantially rod-shaped structures.

70. The device of claim 69, wherein the substrate comprises a material selected from the group consisting of a semiconductor material and a metal.

71. The device of claim 70, wherein the semiconductor material comprises at least one of silicon, amorphous silicon, poly-silicon, silicon carbide and gallium nitride.

72. The device of claim 70, wherein the metal comprises at least one of Al, W and Nb.

73. The device of claim 69, wherein the thickness of the substrate is between about 1 micron and about 550 microns.

74. The device of claim 69, wherein the porous layer comprises an anodized metal oxide.

75. The device of claim 74, wherein the anodized metal oxide comprises at least one of an anodized aluminum oxide and an anodized titanium oxide.

76. The device of claim 69, wherein the thickness of the porous layer is between about 0.5 microns and about 5 microns.

77. The device of claim 69, wherein each of the plurality of substantially cylindrical channels has a diameter of between about 1 nm and about 60 nm.

78. The device of claim 69, wherein each of the plurality of substantially cylindrical channels has a length of between about 0.5 microns and about 5 microns.

79. The device of claim 69, wherein each of the plurality of substantially rod-shaped structures comprises a metal.

80. The device of claim 79, wherein the metal comprises at least one of Pt, Mo, W, Ta, Ir, Mo_2C, HfC, ZrC and NbC.

81. The device of claim 69, wherein each of the plurality of substantially rod-shaped structures comprises a dielectric material.

82. The device of claim 81, wherein the dielectric material comprises at least one metal oxide.

83. The device of claim 82, wherein the at least one metal oxide comprises at least one of TiO, TiO_2, ZnO, ZrO_2, Al_2O_3, Nb_2O_5, $ZrTiO_4$, ZrO_2-Al_2O_3, Al_2O_3-Cr_2O_3, Al_2O_3-TiO_2, TiO_2-RuO_2 and a combination thereof.

84. The device of claim 69, wherein each of the plurality of substantially rod-shaped structures has a diameter of between about 1 nm and about 60 nm.

85. The device of claim 69, wherein each of the plurality of substantially rod-shaped structures has a length of between about 0.1 microns and about 5 microns.

86. The device of claim 69, wherein the gate dielectric layer comprises a material selected from the group consisting of SiO_2, SiN_x, wherein $0.5 \leq x \leq .5$, and Al_2O_3.

87. The device of claim 69, wherein the thickness of the gate dielectric layer is between about 1 nm and about 25nm.

88. The device of claim 69, wherein the conductive layer comprises a material selected from the group consisting of a metal and a semiconductor material.

89. The device of claim 88, wherein the metal comprises at least one of Nb, Pt, Al, W, Mo, Ti, Ni and Cr.

90. The device of claim 88, wherein the semiconductor material comprises at least one of Si, GaN, GaAs and SiC.

91. The device of claim 69, wherein the thickness of the conductive layer is between about 20 nm and about 100 nm.

92. The device of claim 69, wherein the plurality of substantially rod-shaped structures are separated by a distance of between about 50 nm and about 500 nm.

93. The device of claim 69, wherein the self-aligned gated field emission device is suitable for use in an application selected from the group consisting of an x-ray tube application, a flat panel field emission display application, a microwave amplifier application and an electron-beam lithography application.

94. An electronic system, the electronic system having an emissive device, the emissive device comprising at least one self-aligned gated field emission device, wherein the at least one self-aligned gated field emission device comprises:

a substrate having a surface and a predetermined thickness;

a porous layer having a surface and a predetermined thickness disposed adjacent to the surface of the substrate, wherein the porous layer defines a plurality of substantially cylindrical channels, each of the plurality of substantially cylindrical channels aligned substantially parallel to one another and substantially perpendicular to the surface of the substrate;

a plurality of substantially rod-shaped structures disposed within at least a portion of the plurality of substantially cylindrical channels defined by the porous layer and adjacent to the surface of the substrate, wherein a portion of each of the

plurality of substantially rod-shaped structures protrudes above the surface of the porous layer;

a gate dielectric layer having a surface and a predetermined thickness disposed on the surface of the porous layer, wherein the gate dielectric layer is disposed between the plurality of substantially rod-shaped structures; and

a conductive layer having a predetermined thickness selectively disposed on the surface of the gate dielectric layer, wherein the conductive layer is selectively disposed between the plurality of substantially rod-shaped structures.

95. The electronic system of claim 94, wherein the electronic system is an imaging system.

96. The electronic system of claim 95, wherein the imaging system is an x-ray imaging system.

97. The electronic system of claim 94, wherein the electronic system is a lighting system.

98. The electronic system of claim 97, wherein the lighting system is one of a low pressure gas discharge lighting system and a fluorescent lighting system.

99. The electronic system of claim 94, wherein the electronic system comprises at least one of an x-ray source, a flat panel display, a microwave amplifier, a lighting device and an electron-beam lithography device.